ACTIVE CONTAMINATION CONTROL FOR EQUIPMENT AND SUBSTRATES

High-end manufacturing equipment has to support increasing levels of cleanliness. First-tier high-tech system supplier VDL ETG is pro-actively developing capabilities in product design as well as in production process design to support increasing requirements on cleanliness. Where knowledge gaps exist, VDL ETG supports research to further the state-of-art, for example in the ACCESS project: Active Contamination Control for Equipment and SubstrateS. In this project, VDL ETG and Eindhoven University of Technology (TU/e) work together as a multidisciplinary team, to deepen the fundamental understanding of generation, transport and removal of particle contamination.

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Introduction

With constantly increasing requirements on accuracy, productivity and yield, high-end manufacturing equipment has to support increasing levels of cleanliness. Sensitivity for particle, molecular and ionic contamination of advanced processes like semiconductor photolithography and electron microscopy increases with the capability for finer details and higher magnifications. The achievable cleanliness of equipment depends, on the one hand, on specific product design decisions and, on the other hand, on tight cleanliness control of parts manufacturing, assembly and integration processes.

As a tier-1 supplier to many high-end equipment OEMs in semiconductor, analytical, photonic and healthcare industries, VDL ETG, having its own design and engineering capabilities, is pro-actively developing capabilities in product design as well as in production process design to support increasing requirements on cleanliness. Where gaps in knowledge exist, VDL ETG will support research to further the state-of-art, in this case the ACCESS-project. ACCESS is the acronym for Active Contamination Control for Equipment and SubstrateS.

In the ACCESS-project, VDL ETG and various TU/e research groups work together as a multidisciplinary team, to deepen the fundamental understanding of generation, transport and removal of particle contamination. The scale of contamination affects processing of current- and next-generation semiconductor devices, and various kinds of analytical techniques such as electron microscopy, mass spectrometry and spectroscopy.

The project has been designed to be executed by 3 PhD students in combination with 6 PDEng (Professional Doctorate in Engineering) trainees, such that fundamental research activities can be combined with application-driven validation measurements and prototypes.

Background

With scaling continuing in different forms, e.g. shrink according to Moore's law, albeit currently at a reduced pace, and More-than-Moore initiatives such as multiscale packaging and 3D integration, the processes to manufacture semiconductor devices become more and more sensitive. The need for sufficient yield becomes more prominent with increasing sensitivity coupled to increased equipment cost. Also, more process steps become contamination-sensitive. Even more so, increasing the number of layers on a semiconductor wafer (like 3D NAND structures require), increases the susceptibility to contamination. In this highly demanding business environment, it is essential that equipment designers and equipment manufacturers develop deep understanding of particle (and other kinds of) contamination to guarantee sufficient cleanliness and sufficient yield of the production process.

Higher cleanliness reduces the sensitivity for contaminants. Contaminants can be divided into several classes [1]:

1. Particles.
2. Metal ions.
3. Chemicals.
4. Airborne molecular contaminants (AMCs).

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In semiconductors, the presence of contaminants can cause three major defects:

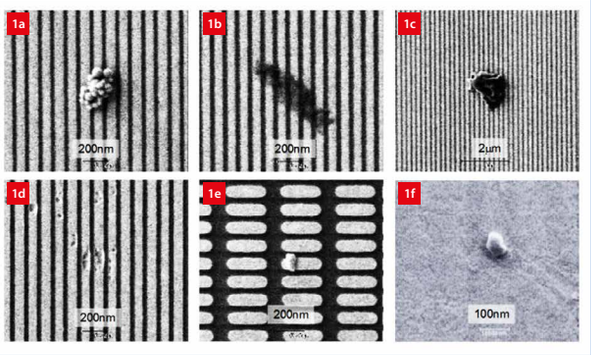
1. Device yield
   This is the most obvious defect and can easily be detected. Contaminants can cause the die to fail electrical tests and thus reduce yield.
2. Device performance
   Contamination can cause a lowering of device performance with time. This is a more serious problem because it causes lowering of device life.
3. Device reliability
   This is the hardest to detect because this can lead to failure, at some point in operational life.

Airborne contaminants (gases and particles) pose serious threats to high-tech industries with the critical dimension of e.g. a microelectronics chip quickly shrinking to nanoscale and the glass substrate of an LCD panel substantially growing to 1.9 m by 2.2 m. In theory, the best strategy to control the contaminants is to locate the emitting origin and to terminate the releasing source. The contaminants mainly originate from two sources: (a) incoming outdoor air, and (b) internal activities (Figure 1). Contamination is the main cause of a killer defect, that is any particle or any crystal defect that causes a disruption in an intended microcircuit pattern

The mechanism of contamination, e.g. in a semiconductor manufacturing environment [3]:

1. The source of contamination.
2. The transportation of the contamination.
3. The location of the contamination: surface, bulk.
4. The evolution of the contamination: how to remove it? Does the cleaning remove the contamination?

In semiconductor equipment, allowed contamination levels depend on productivity. Particle contamination characteristics for high-productivity lithographic equipment



Examples of surface contamination; the common defects induced by post-cleaning [2].
(a) Slurry abrasive particle remains.
(b) Organic residue.
(c) Polisher debris.
(d) Corrosion.
(e) Dendrites.
(f) Small residue defects.

Table 1
Progress over time in particle contamination characteristics for high-productivity lithographic equipment, in terms of particles per wafer pass (PWP) / size.

PWP / size	2015	2018	2022
wafer topside	0.5 / > 60 nm	0.5 / > 40 nm	0.05 / > 20 nm
wafer backside	2,500 / > 0.5 µm	1,750 / > 0.5 µm	600 / > 0.5 µm

are shown in Table 1. For metrology tools in a semiconductor manufacturing environment, having a lower productivity, a lower achievable PWP (particles per wafer pass) has been demonstrated by VDL ETG; 0.08 PWP / > 60 nm. Future requirements, in the next decade, however will even be stricter.

In scientific and analytical equipment, where high electric field strengths are used to generate an image (e.g. the optical path in electron optics), a single particle on a critical location already severely disturbs the image quality due to charging and arcing effects. When higher electric field strengths are implemented, the susceptibility to particle contamination even gets more critical.

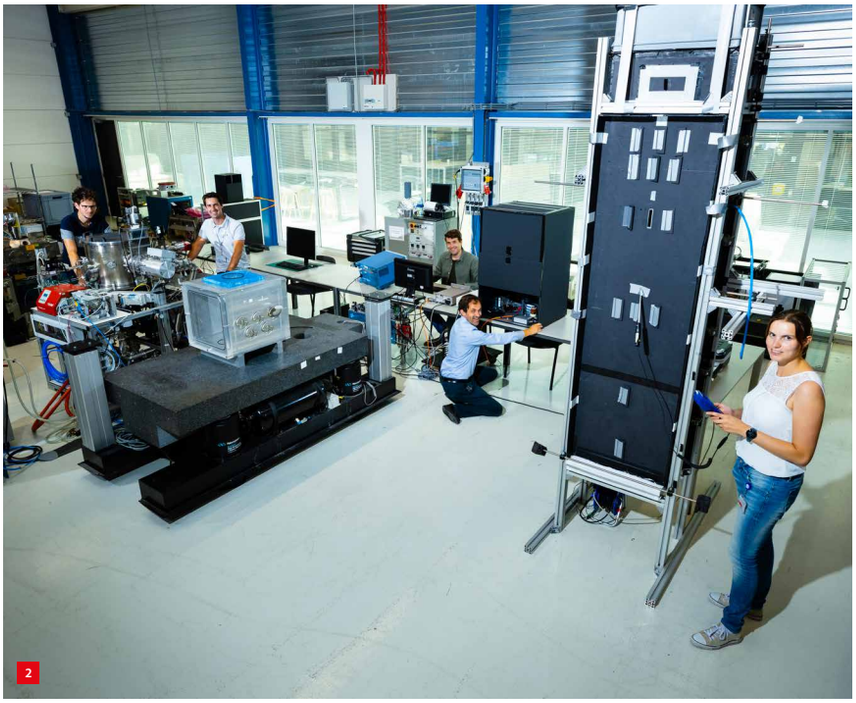
Research approach

The purpose of the ACCESS project is to deepen our fundamental understanding of the (1) generation, (2) transport, and (3) removal of particle contamination. The scale of contamination affects processing of current- and next-generation semiconductor devices, and various kinds of analytical techniques such as electron microscopy, mass spectrometry and spectroscopy.

The work in the ACCESS research projects (see also the following articles) is carried out by three PhD students in various TU/e research groups, namely:

(1) Research project 1: Particle generation
Research group: Mechanics of Materials (Mechanical Engineering department)
(2) Research project 2: Particle transport
Research group: Turbulence and Vortex Dynamics (Applied Physics department)
(3) Research project 3: Particle cleaning
Research group: Elementary Processes in Gas Discharges (Applied Physics department)

Each of the PhD students is assisted by two PDEng trainees to design and build experimental validation tools and prototypes. One of the PDEng trainees works in the Electrical Energy Systems research group at the TU/e Electrical Engineering department. The PhD students and the PDEng trainees are supervised by a technical project leader at the TU/e High Tech System



VDL ETG development lab. (Photo: Bram Saeys)

Center (HTSC) to facilitate the multidisciplinary collaboration between VDL ETG and the various research groups at the TU/e. Supervision by VDL ETG is organised by management under (1) overall supervision of the first author, and (2) various topic leaders with relevant academic backgrounds. Regular meetings and sessions are organised at VDL ETG, where development labs (Figure 2) and project facilities are used for field tests and joint work.

REFERENCES

[1] P. Swaminathan, *Semiconductor Materials, Devices, and Fabrication*, Wiley, ISBN 9788126508624, 2019.

[2] K.-H. Wei, *et al.*, "Cleaning methodology of small residue defect with surfactant in copper chemical mechanical polishing post-cleaning", *Thin Solid Films*, vol. 618, pp. 77-80, 2016.

[3] J. Grym (ed.), *Semiconductor Technologies*, Chapter 4, In-Tech, ISBN 978-953-307-080-3, 2010.

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