How to save over $ 100 mln per year on lithography cost?

Maskless electron beam lithography has emerged as one of the contenders for IC manufacturing. MAPPER's high-throughput solution provides 10 wafers-per-hour exposure units on 1 m² for 22 nm and beyond. This article will explain how such an approach will save IC manufacturers over $ 100 mln per year on lithography cost.

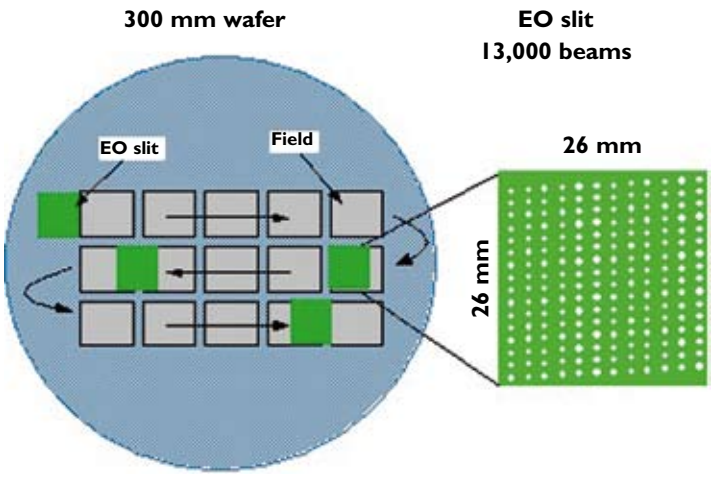
• *Bert Jan Kampherbeek and Marco Wieland* •

Optical lithography today is the leading technology for semiconductor manufacturing. Many technologies have been proposed in the past to replace optical lithography under the assumption that scaling was no longer possible. To date, optical lithography has managed to find solutions to extend the scaling limit – recent examples include low-k1 imaging and double patterning. These innovations however have one major implication: cost. Both lithography tool cost as well as mask (set) cost have risen exponentially to the point that the most advanced optical scanner today costs about € 40 mln and advanced mask set costs of € 2 mln are no rarity. Therefore, if optical lithography is to be replaced with another technology, it will not be so much for performance reasons, but mainly for cost reasons.

High-throughput e-beam solution

Maskless electron beam lithography, or electron beam direct write, has been around for a long time in the semiconductor industry. Mostly this technique has been used for mask writing applications as well as device engineering and in some cases chip manufacturing, thanks to its high resolution and flexibility in changing designs.

However, because of its relatively low throughput compared to optical lithography, electron beam lithography has never been the mainstream lithography technology. MAPPER offers a massively parallel electron beam approach; see Figure 1. This approach eliminates the fundamental throughput limitations of a single-electron beam system by arranging 13,000 parallel electron beams in an optical column no larger than a pack of milk. This



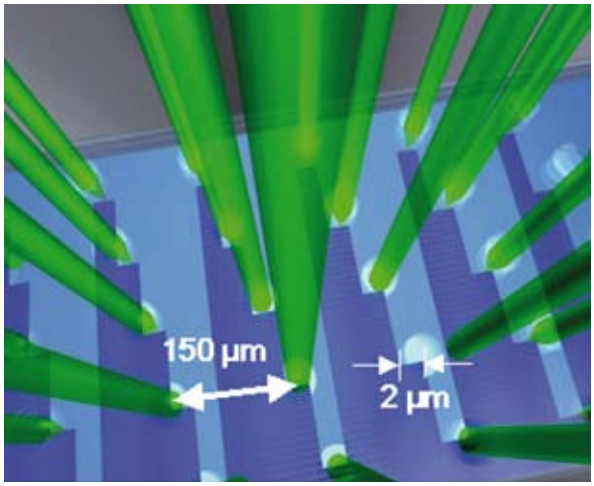


Figure 1. MAPPER's massively parallel electron beam approach.
(a) Arrangement of electron beams and writing strategy.
(b) Zoom of (top view of) beam positions in Electron Optics (EO) slit.

number of beams allows for a 10 wph (wafers per hour) throughput.

The 13,000 electron beams are arranged in an Electron Optics (EO) slit. The beams are on a pitch of 150 µm in such a way that if one looks at the beams from the direction perpendicular to where the slit has a width of 26 mm, the beams are effectively 2 µm apart. The writing strategy is such that complete fields are exposed within one stage scan. The wafer is moved underneath the EO slit from one end of the wafer to the other end; this is done by a wafer stage. Simultaneously to the stage movement, all electron beams are deflected over 2 µm by means of an electrostatic deflector array and the beams are individually switched on and off. In this way a full field can be exposed with only one stage scan, enabling 10 wafers per hour.

The optics that is required to create the array of focused spots is shown in Figure 2. It consists of a single high-brightness cathode run in space-charge limit. An electrostatic collimator lens is used to create a collimated beam. After passing the collimator, the single beam is split up into 13,000 beams by the aperture array. After the aperture array the beamlets are focused by the condenser lens array in the intermediate focus plane. In this plane the beam blanker array is placed that can deflect each individual beam away from a clear aperture on the beam stop array to stop the electrons and switch off the beam at the wafer. After the beam stop array the beams are demagnified by the projection lens array and focused in the wafer plane. A deflector array is positioned between the beam stop array and the projection lens array to scan the beams over a range of 2 µm perpendicular to the wafer stage movement.

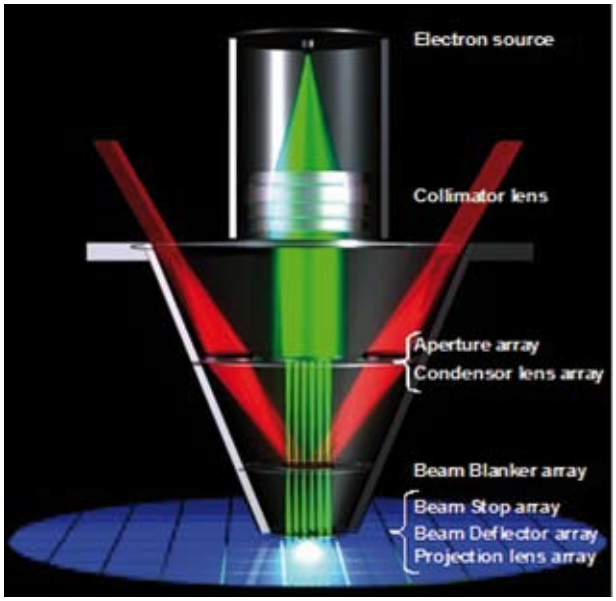


Figure 2. Schematic of MAPPER's massively parallel e-beam column.

System overview and roadmap

MAPPER's machine is capable of 10 wph. This is of course a low productivity compared with an optical scanner. However, throughput is not the only aspect that counts; footprint and tool cost are the two remaining parameters for enabling a competitive cost of ownership. Therefore MAPPER has made a design that enables a footprint of only 1 x 1 m^2 at a selling price of roughly € 5 mln. This creates the opportunity to cluster for example 10 units together to end up with a cluster machine capable of doing 100 wph on a footprint of approximately 15 m^2 or 23 m^2 including service area, which is comparable to today's optical scanners in terms of footprint and cost. Figure 3 shows the current machine with a non-optimized footprint of 1.3 x 1.3 m^2 and how these machines can be grouped in a 100 wph cluster.

Currently, this machine has 110 electron beams capable of exposing 32 nm node patterns [1]. To extend this capability to 10 wafers per hour at the 22 nm node, MAPPER is currently working on a high-speed data path architecture and an upgrade of the optics to 13,000 beams delivering a 150 μA current on the wafer.

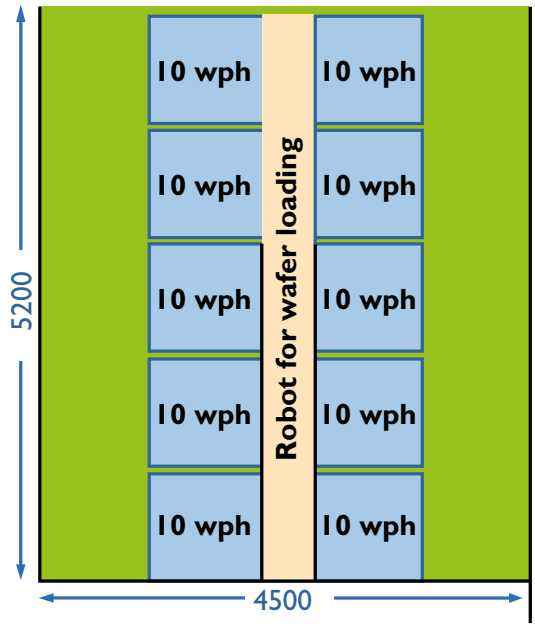


Figure 3. A 100 wph cluster tool.
(a) Schematic.

Comparing lithography technologies on cost

In most discussions about cost different technologies are compared by their cost of ownership (CoO), given by the following equation:

$$\text{CoO [\$ / wafer]} = \frac{\text{tool price [\$]}}{\text{TPT} * 24 * 365 * 5\ \text{[hours]}} + \frac{\text{mask cost [\$]}}{\#\ \text{wafers /design}} + \text{process cost}$$

where TPT = throughput rate (wph), and assuming 100% yield and usage, and 5 years of operation.

The difficult thing about this CoO calculation is that the numbers are different for different products, especially if the mask costs are not to be neglected. Therefore it is a very difficult task for a chip manufacturer to estimate how many wafers are going to be made on average per design, and to be able to judge whether a maskless machine is more favorable or not than a machine needing a mask.

A different look at lithography cost

In the following example, EUV, Double Patterning and MAPPER are compared. The objective is to estimate the total lithography cost for these technologies *per* fab *per* year.

Assume for the purpose of the discussion that all lithography technologies have identical performance, uptime and yield. Let us take a 300 mm wafer fab for 22 nm products with 30,000 wafer starts per month and 15 critical layers to be patterned with one of the three solutions.

(b) The current footprint of a single 300 mm tool.

Assuming a 100% uptime and yield, this means that seven EUV machines at 100 wph are required, seven Double Patterning machines at 200 wph are required and 64 MAPPER machines at 10 wph are required. Following the above mentioned MAPPER tool price and using an estimated price of EUV and Double Patterning

machines of € 40-45 mln and taking into account that the throughput for Double Patterning machines has to be cut in half, this straightforward calculation shows that the capital expenditures for the three technologies are comparable and are roughly € 56-64 mln per year assuming a 5-year depreciation period.

Now what about mask cost?

How many mask sets are required for this 30,000 wafer starts per month per fab? Let us take the example of a best-selling product like Nvidia's GeForce 8800GT / 8800GTS512 / 9800GTX / 9800GX2 family.

In Q3 2008, 111 million GPUs (Graphics Processing Units) were sold [2] and Nvidia had a market share of 27.8% [3]. This means Nvidia made about 31 million GPUs. Assume that about 10% of these GPUs were their most advanced, like the one mentioned previously, this results in 3.1 million GPUs. With a die size of 330 mm^2 [2] and a yield of 90% this comes down to 16,000 wafers per quarter or roughly 5,000 wafers per month.

Therefore, to fill a 30,000 wafer starts per month fab with the world's best-selling products you need about 72 chip designs per year. Taking into account that you need at least two mask sets per design, you end up with 140 mask sets. This represents € 140-280 mln per year for mask sets between € 1-2 mln each. Of course, in reality you need more mask sets than in this example, because there are numerous examples of products that do not end up being a bestseller.

Comparing the € 140 mln number to the amount spent on capital expenditures per year, it is obvious that mask costs are far more important for a Logic IC manufacturer than the cost of hardware.
This comparison will not hold for memory and microprocessors since the number of mask sets required per year will be lower. However, even for these IC manufacturers the mask set cost will be at least comparable to the capital expenditures, and thus maskless lithography will result in a cost reduction of at least 50%.

Conclusions

MAPPER is developing a massively parallel electron beam direct write system. Even at relatively low throughputs of 10 wph per machine this solution is cost effective for semiconductor manufacturing, because of:

- small footprint of ~1 m^2 per exposure unit;
- low system price;
- possibility of clustering several exposure units together;
- no mask cost, saving the IC manufacturers hundreds of millions per year.

Authors' note

Bert Jan Kampherbeek received his Masters degree in Applied Physics in 1999 at Delft University of Technology in the field of Electron Optics. He is one of the three founders of MAPPER Lithography and currently holds the position of VP Market Development.
Marco Wieland received his Masters degree in Applied Physics in 1999 at Delft University of Technology in the field of Electron Optics. He is one of the three founders of MAPPER Lithography and currently holds the position of VP Research & Development. Marco holds over thirty patents.

References

[1] M. J. Wieland, G. de Boer, G. F. ten Berge, et al., MAPPER: High Throughput Maskless Lithography, SPIE Proceedings 2009.
[2] www.tgdaily.com/content/view/37554/135
[3] www.tomshardware.com/news/GPU-videocard-Nvidia-AMD,6533.html

Information

www.mapperlithography.com